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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/018,783	02/04/1998	THOMAS L. RITZDORF	11928US01	1242

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EXAMINER	
MAGEE, THOMAS J	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/018,783	RITZDORF ET AL.	
	Examiner	Art Unit	
	Thomas J. Magee	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-31 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 29 is objected to for the lack of antecedent precedent. There is no *"step of removing the copper metallization ... using a chemical mechanical polish technique"* disclosed in Claim 24. Correction is required.

Claim Rejections – 35 U.S.C. 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 2, 6, 7, 24 – 26, and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Ding et al. (US 6,066,892).

4. Regarding Claims 1, 2, 6, and 7, Ding et al. disclose a method for filling recessed microstructures at a surface of a semiconductor workpiece with metallization (Cu) com-

prising the steps of depositing a metal (Cu) layer (62) (Figure 3) into the microstructure (56) with a process (electroplating) to generate small grains sufficient to fill the structure, (Col. 5, lines 59 – 66) (Figure 3)

5. Regarding Claims 24 – 26, Ding et al. disclose a method for filling recessed micro-structures at a surface of a semiconductor workpiece with Cu metallization, comprising providing a semiconductor workpiece with a feature that is to be connected with Cu metallization (Figure 3), wherein at least one dielectric layer (54) is present over the surface of the semiconductor workpiece, including the feature, with a recessed micro-structure (56) within the dielectric layer. Ding et al. further disclose that the surface is "prepared" for the subsequent Cu deposition by depositing a seed layer (60) which serves as a barrier and adhesion layer (Col. 6, lines 52 – 56), whereupon, a Cu layer (62) is deposited to substantially fill the recessed micro-structure and the layer followed by annealing at no more than 100 degrees (C) (Col. 6, lines 19 – 20).

6. Regarding Claim 28, Ding et al. disclose (Col. 5, lines 64 – 66) that the Cu seed layer may be formed by PVD (sputtering) (Col.5, lines 35 – 37).

Claim Rejections – 35 U.S.C. 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office Action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ding et

al., as applied to Claims 1, 2, 6, 7, 24 – 26, and 28, and further in view of Dubin et al. (US 5,972,192).

9. Regarding Claims 3 and 8, Ding et al. do not disclose that an electroplating waveform is used, at least in part, to ensure that sufficiently small grain size is present so that the recessed microstructure is appropriately filled. Dubin et al. disclose (Col. 9, line 55 through Col.10, line 7; Col. 10, lines 22 – 27, lines 44 – 47; Col. 4, line 62 through Col.5, line 7) an electroplating waveform, wherein the metal (copper) is deposited in the recess of an appropriate grain size to fill the recess. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Dubin et al. with Ding et al. to obtain adequate filling of vias and trenches.

10. Claims 4 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ding et al., as applied to Claims 1, 2, 6, 7, 24 – 26, and 28, and further in view of Cope (US 3,715,289).

11. Regarding Claims 4 and 9, Ding et al. do not disclose that an electroplating solution additive is used, at least in part, to ensure sufficiently small grain size. Cope discloses (Col. 1, lines 5 – 17; Col. 1, line 43 through Col. 2, line 15) that the addition of certain additives produces an improvement in grain size, as well as a number of other properties. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Cope with Ding et al. to obtain controlled small grain nucleation within recesses of the microstructure.

12. Claims 5 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ding et al., as applied to Claims 1, 2, 6, 7, 24 – 26, and 28, and further in view of Tomov et al. ("Recovery and Recrystallization of Electrodeposited Bright Copper Coatings at Room Temperature II: X-Ray Investigation of Primary Recrystallization," Journ. of Applied Electrochemistry, Vol. 15, (1985), pp. 887 – 894).

13. Regarding Claims 5 and 10, Ding et al. do not disclose a room temperature annealing process. Tomov et al. disclose (Abstract) that the growth and recrystallization of grains in electrodeposited coatings occurs at room temperature (Figures 5a), 6a)). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Tomov et al. with Ding et al. to obtain annealed films of appropriate physical properties (Intro., second para., p. 887, Tomov et al.) for use in a device.

14. Claims 11 - 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ding et al., as applied to Claims 1, 2, 6, 7, 24 – 26, and 28, and further in view of Tomov et al., and Chen et al. (5,989,623).

15. Regarding Claims 11, 13, 16 – 20, and 23, Ding et al. disclose a method for filling recessed micro-structures at a surface of a semiconductor workpiece with Cu metallization, comprising providing a semiconductor workpiece with a feature that is to be connected with Cu metallization (Figure 3), wherein at least one dielectric layer (54) is present over the surface of the semiconductor workpiece, including the feature, with a recessed micro-structure (56) within the dielectric layer. Ding et al. further disclose that the surface is "prepared" for the subsequent Cu deposition by depositing a seed layer (60) which

serves as a barrier and adhesion layer (Col. 6, lines 52 – 56), whereupon, a Cu layer (62) is deposited to substantially fill the recessed micro-structure.

Ding et al. do not disclose the room temperature annealing of the copper. As discussed previously, Tomov et al. disclose the room temperature annealing of electrodeposited films for fixed periods of time. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Tomov et al. with Ding et al. to obtain annealed films of appropriate physical properties (Intro., second para., p. 887, Tomov et al.) for use in a device.

Additionally, Ding et al. do not disclose the removal of Cu metallization from the surface after annealing. Chen et al. disclose the (cmp) removal of Cu metallization from the workpiece (Col. 8, lines 33 – 39). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Chen et al. with Ding et al. to obtain a removal/ planarization process for the Cu layer on the workpiece.

16. Regarding Claim 12, Ding et al. do not disclose room temperature annealing or a time period for such annealing. Tomov et al. disclose (Figure 6a) a period exceeding 20 hours for annealing in order to achieve stabilization. It would have been obvious to combine Tomov et al. with Ding et al. to obtain a stabilized film of appropriate physical properties.

17. Regarding Claims 15 and 22, Ding et al. disclose (Col. 5, lines 64 – 66) that the Cu seed layer may be formed by PVD (sputtering) (Col.5, lines 35 – 37).

18. Regarding Claims 14 and 21, Ding et al. do not disclose the use of CVD for

formation of the Cu seed layer. Chen et al. disclose the use of CVD to form a Cu seed layer (92) (Figure 5b) for increased adhesion and decreased surface roughness. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Chen et al. with Ding et al. to obtain a seed layer with improved adherence with the overlying fill layer.

19. Claims 27 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ding et al., as applied to Claims 1, 2, 6, 7, 24 – 26, and 28, and further in view of Chen et al.

20. Regarding Claim 27, Ding et al. do not disclose the use of CVD for formation of the Cu seed layer. Chen et al. disclose the use of CVD to form a Cu seed layer (92) (Figure 5b) for increased adhesion and decreased surface roughness. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Chen et al. with Ding et al. to obtain a seed layer with improved adherence with the overlying fill layer.

21. Regarding Claim 29, Ding et al. do not disclose the removal of Cu metallization from the surface after annealing. Chen et al. disclose the (cmp) removal of Cu metallization from the workpiece (Col. 8, lines 33 – 39). It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Chen et al. with Ding et al. to obtain a removal/planarization process for the Cu layer on the workpiece.

22. Claims 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Chen et al. in view of Wolf ("Silicon Processing for the VLSI Era, Vol. 4: Deep Submicron Process Technology," Lattice Press, Sunset Beach, CA (2002), pp. 639 – 670).

23. Regarding Claims 30 and 31, Chen et al. disclose a method for filling recessed micro-structures at a surface of a semiconductor workpiece with Cu metallization, comprising a semiconductor workpiece (40) (Figure 5A) that is to be connected with Cu metallization, applying a low-k dielectric layer (Col. 5, line 66 through Col. 6, line 2) (42) over a surface of the workpiece, including the feature (46), wherein a recess (48) is provided in the di-electric layer and a seed layer (92) applied on the surface in preparation for the electro-chemical deposition of the Cu layer (62) (Figure 5D) to fill the recess. Chen et al. further disclose (Col. 10, lines 54 – 62) that the electrochemically deposited layer is subjected to a self annealing process during deposition with a substrate temperature of 150 degrees (C). Chen et al. do not disclose the degradation temperature or bake temperature for the low-k layer. However, Wolf discloses the desireable material properties of low-k films for compati-bility in IC processing (Table 14-4). Thermal stability at approximately 400 degrees (C) is considered optimal for a wide class of low-k materials. Hence, temperatures of 150 degrees (C) in self annealing of electrochemically deposited Cu films would be below the degradation or bake temperature of low-k films. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine a summary of materials properties of low-k films, as disclosed by Wolf, with Chen et al. to ascertain compatibility with Cu anneal-ing steps.

Conclusions

24. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to **Thomas Magee**, whose telephone number is **(571) 272 1658.** The Examiner can normally be reached on Monday through Friday from 8:30AM to 5:00PM (EST). If attempts to reach the Examiner by telephone are unsuccessful, the examiner's supervisor, **Eddie Lee**, can be reached on **(571) 272-1732.** The fax number for the organization where this application or proceeding is assigned is **(703) 872-9306.**

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Thomas Magee
February 2, 2004